(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 July 2004 (22.07.2004)

PCT

(10) International Publication Number
WO 2004/061724 A1

(51) International Patent Classification[7]: G06F 17/50

(21) International Application Number:
PCT/US2002/040428

(22) International Filing Date:
17 December 2002 (17.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NJ 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ARTHANARI, Geetha** [IN/US]; 38 Thasha Lane, I-4, Essex Junction, VT 05452 (US). **CARRIG, Keith, M.** [US/US]; 74 South Street, Unit E, Essex Junction, VT 05452 (US). **LASHER, Mark, R.** [US/US]; 146 Lindale Drive, Colchester, VT 05446 (US). **MENARD, Daniel, R.** [US/US]; 9 Acton Street, Arlington, MA 02476 (US).

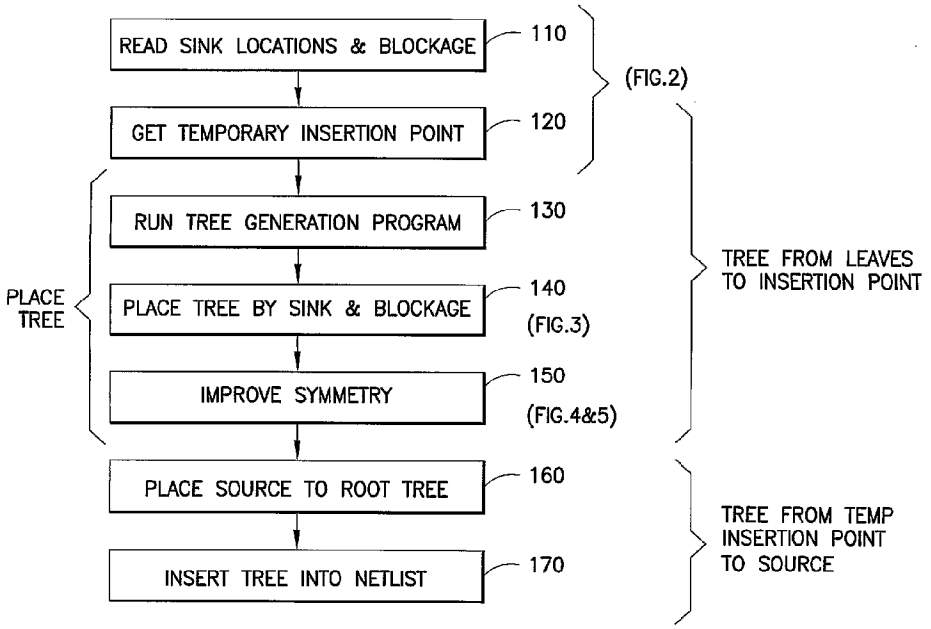
(74) Agent: **NEFF, Daryl, K.**; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: ASIC CLOCK FLOOR PLANNING METHOD AND STRUCTURE



(57) Abstract: A method of designing a clock tree in an integrated circuit combines steps of making a list of all clock sinks (110); positioning a temporary reference insertion point (TIP) (120); grouping the sinks together with structured clock buffers (SCBs) in a set of levels (140); and moving the SCBs to improve symmetry of the tree (150). The SCBs may be of several sizes and may be positioned horizontally (42) or vertically (45) and moved within limits (46) to permit the program to calculate a complete tree.

WO 2004/061724 A1

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ASIC CLOCK FLOOR PLANNING METHOD AND STRUCTURE

Technical Field

The field of the invention is that of designing and constructing a clock tree in an integrated circuit.

Background Art

In the field of integrated circuits, a constant need is that of distributing the clock signal. As clock speeds have increased, the tolerances on clock skew have tightened.

A number of commercial products are on the market to assist in the design process. Cadence offers a program, Clock Tree Synthesis (TM), which generates a tree with limits on the size of a buffer and/or on the complexity of the floor plan that the tree can accommodate. Synopsis offers a program, Clock Tree Compiler (TM) that is generally similar.

IBM has a program, using a method described in U.S. Patent 6204713, which can handle large buffers, which permits a tree with fewer levels.

The problem in generating clock trees can be described generally as striking a balance between delay, power consumed and ability to accommodate circuit blocks that have had their designs frozen. A short delay in the clock chain helps control skew. Low power is always desirable and the ability to re-use predesigned circuit blocks (embedded processors, RAMs, I/O, etc.) without redoing the layout to accommodate the clock saves greatly on cost in developing an ASIC.

Disclosure of the Invention

The invention relates to a method of designing a clock tree that accommodates an existing layout while selecting clock buffer size and orientation to match the floorplan.

Accordingly, a method and corresponding article of manufacture are provided for designing a clock tree in an integrated circuit comprising:

collecting a set of sink locations 3 in a master list and a set of blocked areas 47;

(a) selecting a temporary insertion point (TIP) 4, 5;

(b) enclosing the sink 41 at the first level furthest from the TIP in a bin 40 that includes a first subset of sinks 43 and remove the first subset from the master list;

(c) assigning a first-level structured clock buffer (SCB) 42 to the bin;

repeating steps (a), (b) and (c) above for the remaining sinks in the first level of buffers and subsequent levels until the root level is reached;

improving the symmetry of the tree by moving SCB 45 locations within constraints 46 to concentrate SCBs in rows and columns;

connecting the root level TIP 610 to lower levels; and

connecting a source (S) of clock signals to the root level TIP.

Brief Description of The Drawings

Figure 1 lists steps in a preferred embodiment of the invention.

Figure 2 shows a sample set of sink locations.

Figure 3 shows an example of grouping the sinks in bins served by a buffer.

Figures 4 and 5 show initial and final locations of a set of buffers.

Figure 6 shows a completed tree.

Best Mode for Carrying Out the Invention

The invention is intended to be used in the design of integrated circuits, especially ASICs, where a short design process is an important part of keeping costs down. In the course of designing large-scale (30,000,000+ gates) ASICs, the process of routing the clock tree around the pre-designed modules that form the bulk of the ASIC consumes a significant amount of time and cost.

Among advantages that may arise by application of the invention are the following:

-automatic or manual selection of a reference point (or temporary insertion point (TIP)) that starts the branching process;

-flexibility in range and aspect ratio of buffers;

-choice of either one or both of top-down or bottom-up methods;

-provision of trees having buffers of different sizes;

-allowance for the user to intervene in the design;

The sequence of steps according to a preferred embodiment of the invention is:

collect the clock sink locations and blockage dimensions.

pick the TIP for the lowest (leaf) level

group the sinks in bins, starting with the one furthest from the TIP and place a first-level buffer in each bin

pick a TIP for the first level

group the first-level buffers in bins, starting with the one furthest from the TIP and place a second-level buffer in each bin

repeat the TIP selection and binning step until the root level is reached

improve the symmetry by moving buffers within constraints to concentrate buffers in rows and columns

add buffers from the source to the TIP, and

insert the tree in the netlist.

Figure 2 illustrates a simplified example of an integrated circuit being processed according to the invention. At the center of the figure, filled rectangle 1 represents the TIP. Hollow rectangles 3 represent clock sinks, which is a general term for the interface between the tree and the logic. The logic surrounding the interface points is omitted for clarity in presentation. The diamond on the left side represents the source of the clock signals. Capital C, 4, represents a point calculated by taking the mean between the extreme coordinates of all the sinks - e.g. x = (xmax + xmin)/2 and y = (ymax + ymin)/2. The capital C', 5, represents the centroid calculated by taking the mean of all the sink coordinates. These sinks will be grouped and assigned to a buffer that distributes the clock signal.

Buffers according to the invention, referred to as structured clock buffers (SCBs) are circuits built of N parallel kernels along an axis, where N is greater than or equal to one. These buffers can be inverting or Non-Inverting. Outputs of the kernel are tied together. Balanced wiring is used to wire the circuits of the Structured Clock Buffers. U.S. Patent 6204713, incorporated by

reference, explains the design and construction of such buffers.

It is an advantageous feature of the invention that the buffers are not restricted to a layout along a single axis (horizontal or vertical) but that layout along both axes may be provided, in order to permit a buffer to fit in a limited space. As those skilled in the art are aware, circuit layout is conventionally done with the axis of the transistors lined with one of the coordinate directions.

Designing a vertical buffer that fits within a layout that was intended to be horizontal is non-trivial and requires that the transistors in the vertical SCBs must be in same orientation as the horizontal SCBs. In addition, balanced wiring is needed for both orientations. Power rings are needed for either the vertical or horizontal SCB to account for differences in the vertical or horizontal power distribution. This may require an additional wiring level for vertical or horizontal SCBs in order to fit in additional wires. Layouts are modified so that each horizontal SCB has a delay and output drive capability that match a corresponding vertical SCB.

The TIP can be calculated automatically by calculating the delay, power and placability at the center of the sinks (C), the centroid of the sinks (C') and at a set of intermediate points between C and C'. The selection rule is summarized as: If the center of the sinks is closer to the source than the centroid is, then the TIP is placed at the center. If there is a block (a module that cannot be re-drawn) at the center, then the TIP is placed at a different location, either the centroid or at one of the intermediate points between the center and the centroid.

The placability algorithm produces a result of zero if the location is blocked. The best score is generated by an unblocked location large enough for the SCB, and closest to the desired placement point. The score decreases as the distance from the desired point increases, reflecting the undesirability of additional distance.

The TIP point can be determined by calculating a score that is the sum S1W1 + S2W2 + S3W3, where S1, S2 and S3 are 0 or 1, depending on which

aspect the designer wishes to emphasize and W1 = K1*Delay, W2 = K2*Power and W3 = K3*Placability, where Ki is determined empirically

Once the TIP has been placed, the sinks at the lowest level of the clock tree are grouped. A rectangle (bin) is placed, just enclosing the sink farthest from the TIP. The initial size of the bin is set empirically, based on experience with the density of sinks. The bin may be adjusted up or down to approach the desired size. Illustratively, a bin holding about 20 The actual number is determined by the drive capability of the SCB and the wiring delays to get to the sinks.

Similarly, the number of levels in the tree will be set empirically, e.g. at three. Again the actual number is determined by the drive capability of the SCB and the wiring delay's to get to the sinks. More levels can be added for larger trees.

A buffer is placed at the center of the rectangle, which may be moved slightly in the x and/or y directions to accommodate the maximum number of sinks. The size of the buffer is set to be able to drive the sinks in the bin. It is an advantageous feature of the invention that the size of the buffers may be selected from a set of pre-designed buffers in order to drive the number of sinks that happen to be in the bin, rather than cutting down the size of the bin to accommodate the buffer. The sinks included in that bin are deleted from the master list of sinks and the next bin is placed.

Fig 3 has been drawn to illustrate a situation in which a pair of modules 45 and 47 are located such that a horizontal buffer will not fit. According to the invention, the buffer is moved toward the TIP to try to find a location that fits and still permits the buffer to drive the sinks. If such a location is not found, a vertical buffer is placed. If a vertical buffer will not fit, the program places a horizontal buffer in the original location, even if it is overlapping fixed blocks, printing a warning message for the user to correct it manually. Such a situation is illustrated with buffer 42. The sequence is that the program will exhaust the possibilities in the horizontal, and then exhaust the possibilities in the vertical then warn the user if no placement is possible.

Referring now to Fig 3, there is shown a set of three SCB areas represented by boxes 20, 30 and 40 holding sink subsets 23, 33 and 43 and positioned around SCBs 22, 32 and 42, respectively. The dimensions of a box represent the distance over which a clock signal can be transmitted by the SCB at the center of the box within the restrictions on skew, etc. set by the circuit designer. Illustratively, the boxes have been shifted to have a boundary that is next to the extreme position of a sink - i.e. box 20 has been placed so that the sink 21, furthest from the TIP is at its edge; similarly for box 30 and sink 31 and for box 40 and sink 41.

According to the invention, the size of the SCB will be set to drive the sinks within its range. It is an advantageous feature of the invention that the size of a buffer is flexible.

Once the first bin is set, the sink remaining in the master list that is furthest from the TIP is located and a bin is placed enclosing it. The preceding procedure is repeated until all the sinks have been placed in bins. This covers the leaf level of the clock tree.

The binning procedure is repeated, using first and second level buffers in place of leaf-level sinks, until the root level of the tree is reached.

Once the sinks have been allocated to SCBs, a process of improving the symmetry of the tree can be performed. Fig. 4 shows a simplified example of a layout in which three SCBs 142, have been fixed for one reason or another and will not be moved in this step. Examples of a fixed SCB may be a customer pre-placing and assigning one SCB to some high speed critical circuits (i.e. high speed interface). Another case might be one where part of the chip already meets the timing requirements and the customer does not wish to revisit the compromises made to get that result.

Blocks 47 represent layout modules that will not be moved. The clock tree must be routed around them. The other SCBs, labeled 45, can be moved. In this example, there is a 10x10 grid and a rule that an SCB can be moved by only one step vertically or horizontally. Possible moves are indicated by the arrows.

The principle of the move is to concentrate SCBs on the same row or column, thereby providing a more compact distribution net and simplifying skew and latency.

The procedure followed is to calculate, for each row and column, the number of SCBs in that row or column, and the number that could be included within the rules. The numbers on the side and bottom indicate the actual number and potential number of SCBs in that row or column.

Fig. 5 shows the final configuration of SCBs after allowed moves have been made. The effect of the moves has been to concentrate the horizontal distribution in four rows, with the vertical distribution being spread more broadly.

Fig. 6 shows the result of connecting the SCBs from Fig. 5. Leaf-level buffers are denoted with numeral 630. Second-level buffers are denoted with numeral 620 (located in the middle, about one third from the bottom and from the top). The root level buffer is denoted with numeral 610, located at the center. Location of the root at or near the center is not required, though it contributes to symmetry and a compact layout. The location of the source is not shown in this Figure. It will be located at a fixed position and a route constructed from it to SCB 610.

The temporary insertion point, which is used in each level of the clock tree looks at both its sink circuits (bottom of tree) and the source circuit for those sinks (top of tree).

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

Industrial Applicability

The invention has applicability to the design and fabrication of integrated electronic circuits.

Claims

What is claimed is:

1. A method of designing a clock tree in an integrated circuit comprising the steps of:

collecting a set of sink locations 3 in a master list and a set of blocked areas 47;

(a) selecting a temporary insertion point (TIP) 4, 5;

(b) enclosing the sink 41 at the first level furthest from the TIP in a bin 40 that includes a first subset of sinks 43 and remove the first subset from the master list;

(c) assigning a first-level structured clock buffer (SCB) 42 to the bin;

repeating steps (a), (b) and (c) above for the remaining sinks in the first level of buffers and subsequent levels until the root level is reached;

improving the symmetry of the tree by moving SCB 45 locations within constraints 46 to concentrate SCBs in rows and columns;

connecting the root level TIP 610 to lower levels; and

connecting a source (S) of clock signals to the root level TIP.

2. A method according to claim 1, in which said step (a) of selecting a TIP (4,5) comprises calculating a center 4 of sinks and a centroid 5 of sinks and automatically placing said TIP at one of said center, centroid or an intermediate point between said center and centroid in accordance with an algorithm that locates available space.

3. A method according to claim 2, in which said step (a) of selecting a TIP (4,5) comprises calculating a center 4 of sinks and a centroid 5 of sinks and

automatically placing said TIP at one of said center 4, centroid 5 or an intermediate point between said center and centroid in accordance with an algorithm that locates selectively weights one or more of delay, power consumed and placability.

4. A method according to claim 1, in which said step (c) of assigning a first-level SCB 42 to the bin comprises steps of attempting to place a horizontal SCB 42, then attempting to place a vertical SCB 42 in a central location when a horizontal SCB will not fit in said central location.

5. A method according to claim 4, in which said vertical SCB comprises a set of circuit elements laid out to have substantially the same delay as a corresponding SCB with horizontal layout.

6. A method according to claim 1, in which said step of improving symmetry comprises a step of calculating for each of a set of columns and rows a potential improvement in symmetry of SCBs 45 in an nth level of said tree and moving SCBs 45 to improve symmetry.

7. A method according to claim 6, in which some designated SCBs 142 are excluded from the calculation in said step of improving symmetry, whereby only a subset 45 of SCBs are included in the calculation.

8. A method according to claim 6, in which the amount of movement permitted to improve symmetry 46 is restricted to a preset amount.

9. A method according to claim 1, in which said SCB 42 assigned to a subset of sinks is selected from a set of predesigned SCBs of varying capacity.

10. An article of manufacture in computer readable form which encodes a set of instructions for performing a method according to any of claim 1 through claim 9.

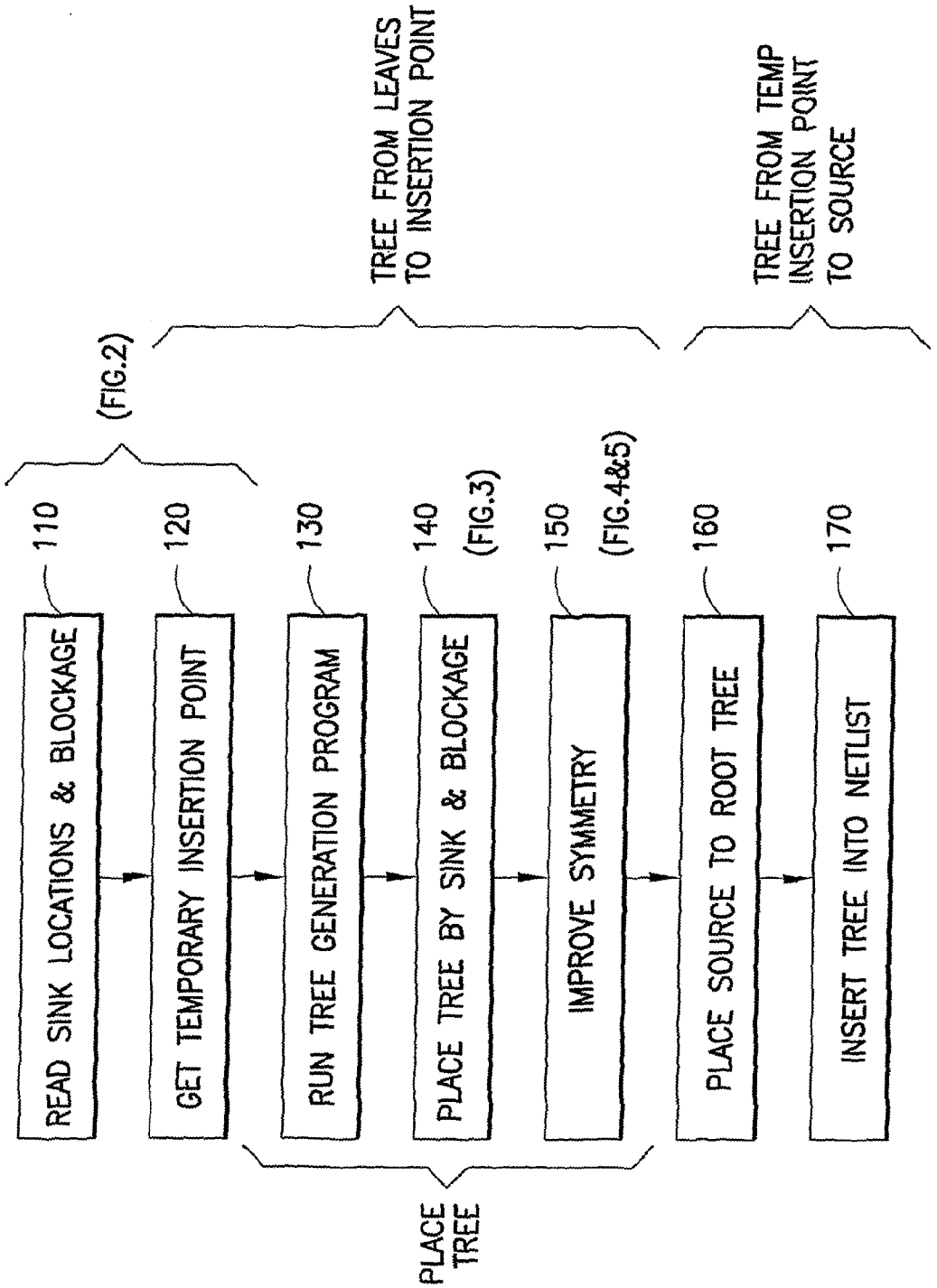

TREE FROM LEAVES TO INSERTION POINT
TREE FROM TEMP INSERTION POINT TO SOURCE
(FIG.2)
110
READ SINK LOCATIONS & BLOCKAGE
120
GET TEMPORARY INSERTION POINT
130
RUN TREE GENERATION PROGRAM
140
(FIG.3)
PLACE TREE BY SINK & BLOCKAGE
150
(FIG.4&5)
IMPROVE SYMMETRY
160
PLACE SOURCE TO ROOT TREE
170
INSERT TREE INTO NETLIST
PLACE TREE

FIG.1

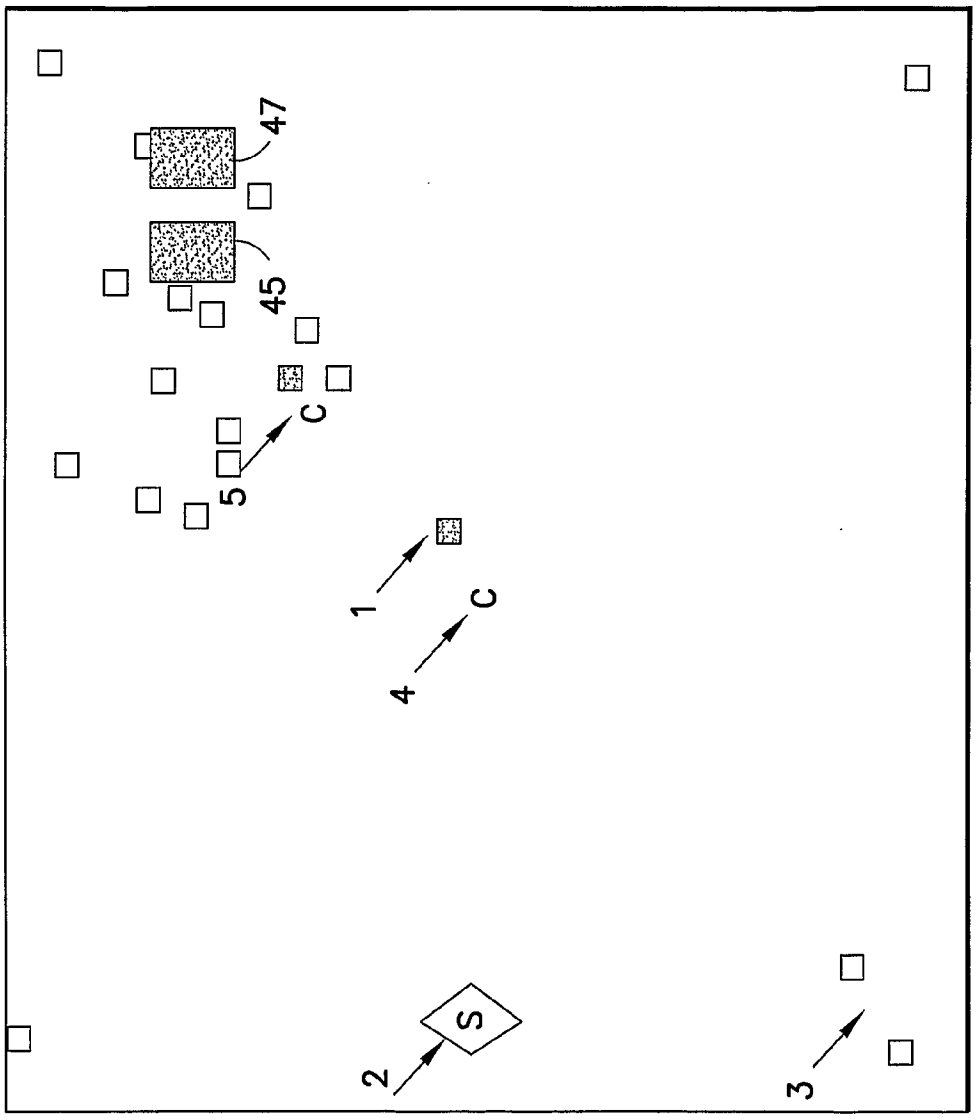


FIG.2

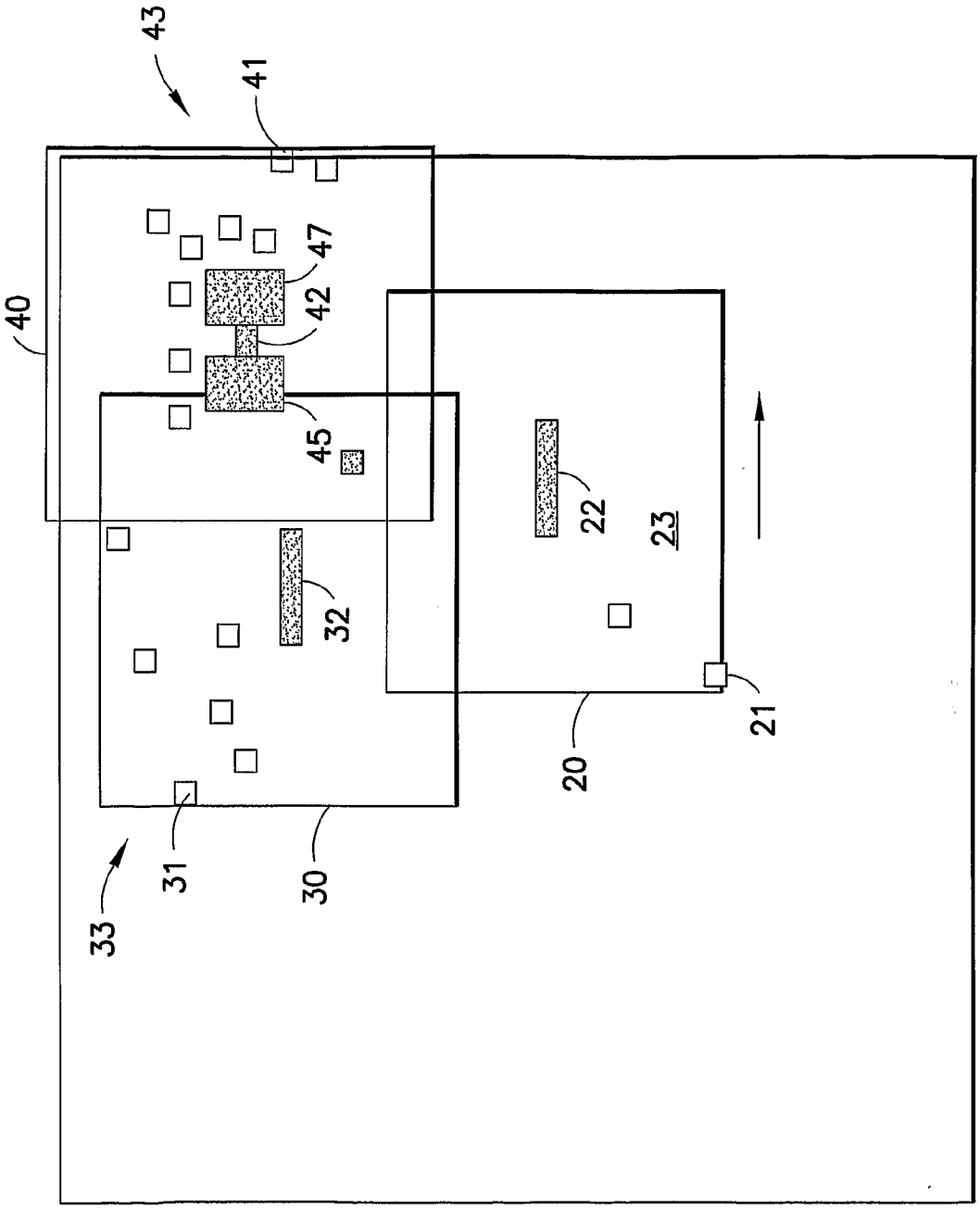


FIG.3

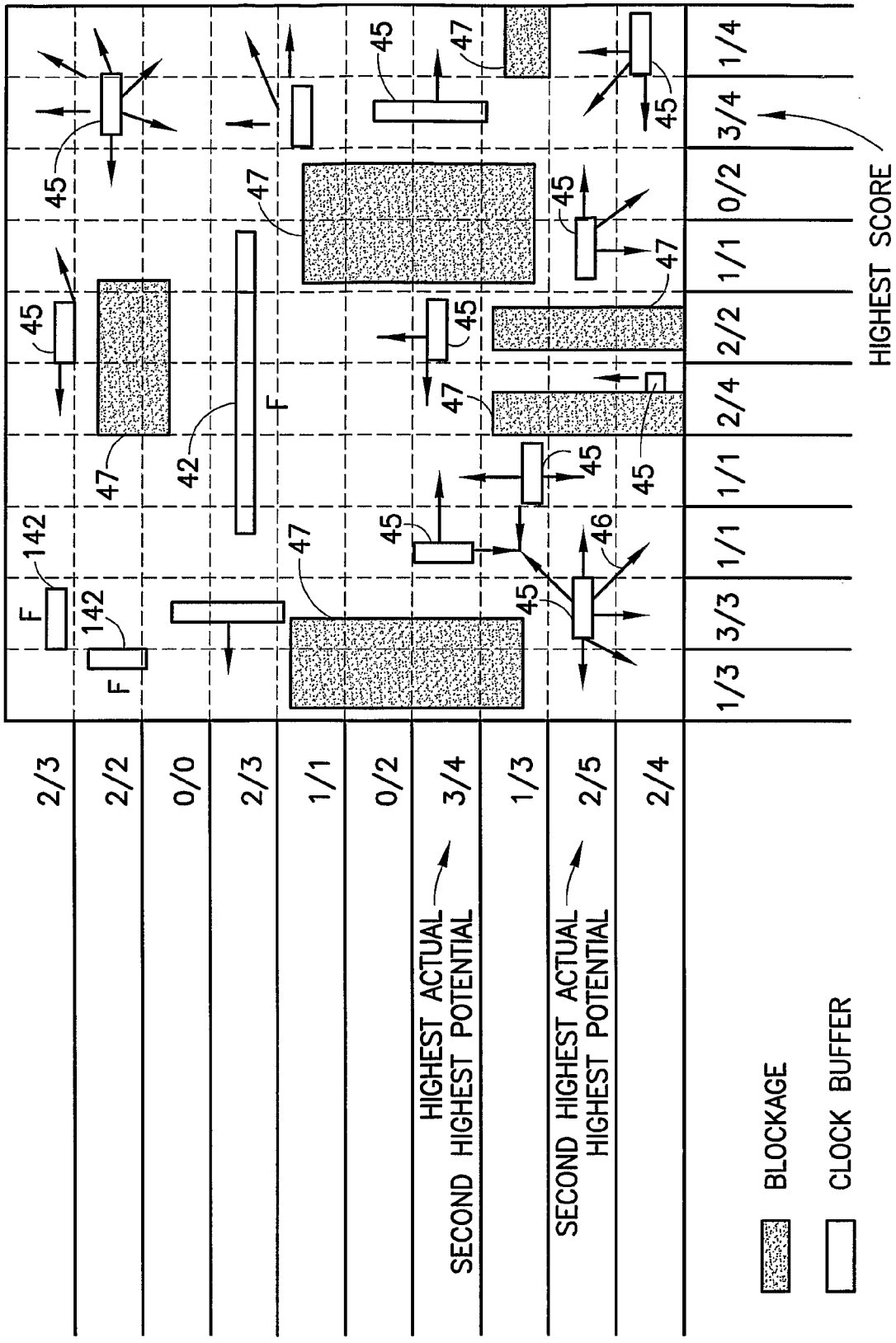

2/3
2/2
0/0
2/3
1/1
0/2
HIGHEST ACTUAL
SECOND HIGHEST POTENTIAL
3/4
1/3
SECOND HIGHEST ACTUAL
HIGHEST POTENTIAL
2/5
2/4
1/3
3/3
1/1
1/1
2/4
2/2
1/1
0/2
3/4
1/4
HIGHEST SCORE
BLOCKAGE
CLOCK BUFFER
F
142
42
45
46
47

FIG.4

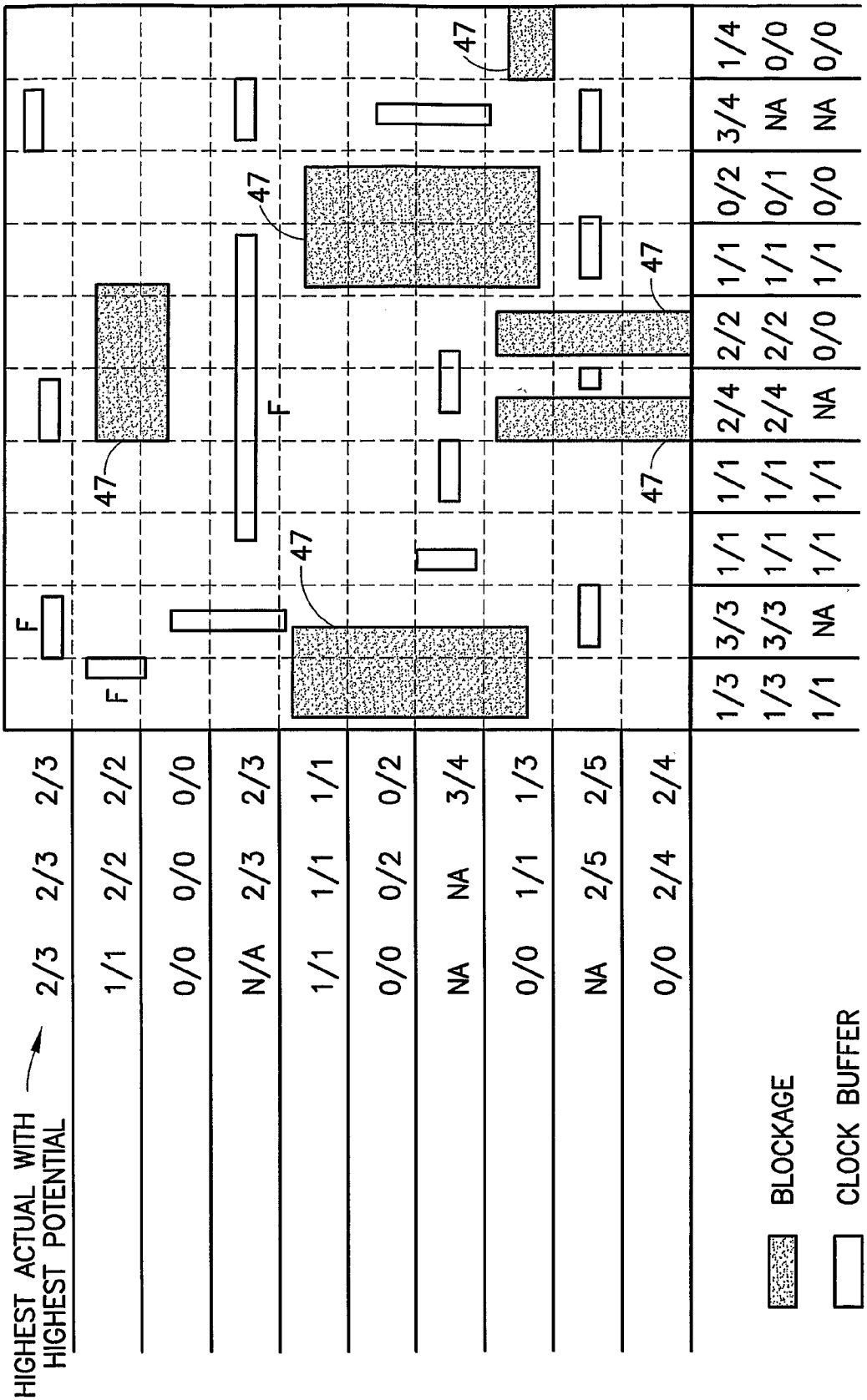

HIGHEST ACTUAL WITH HIGHEST POTENTIAL
2/3 2/3 2/3
1/1 2/2 2/2
0/0 0/0 0/0
N/A 2/3 2/3
1/1 1/1 1/1
0/0 0/2 0/2
NA NA 3/4
0/0 1/1 1/3
NA 2/5 2/5
0/0 2/4 2/4
1/3 3/3 1/1 1/1 2/4 2/2 1/1 0/2 3/4 1/4
1/3 3/3 1/1 1/1 2/4 2/2 1/1 0/1 NA 0/0
1/1 NA 1/1 1/1 NA 0/0 1/1 0/0 NA 0/0
F
47
BLOCKAGE
CLOCK BUFFER
NO MORE MOVES AVAILABLE

FIG.5

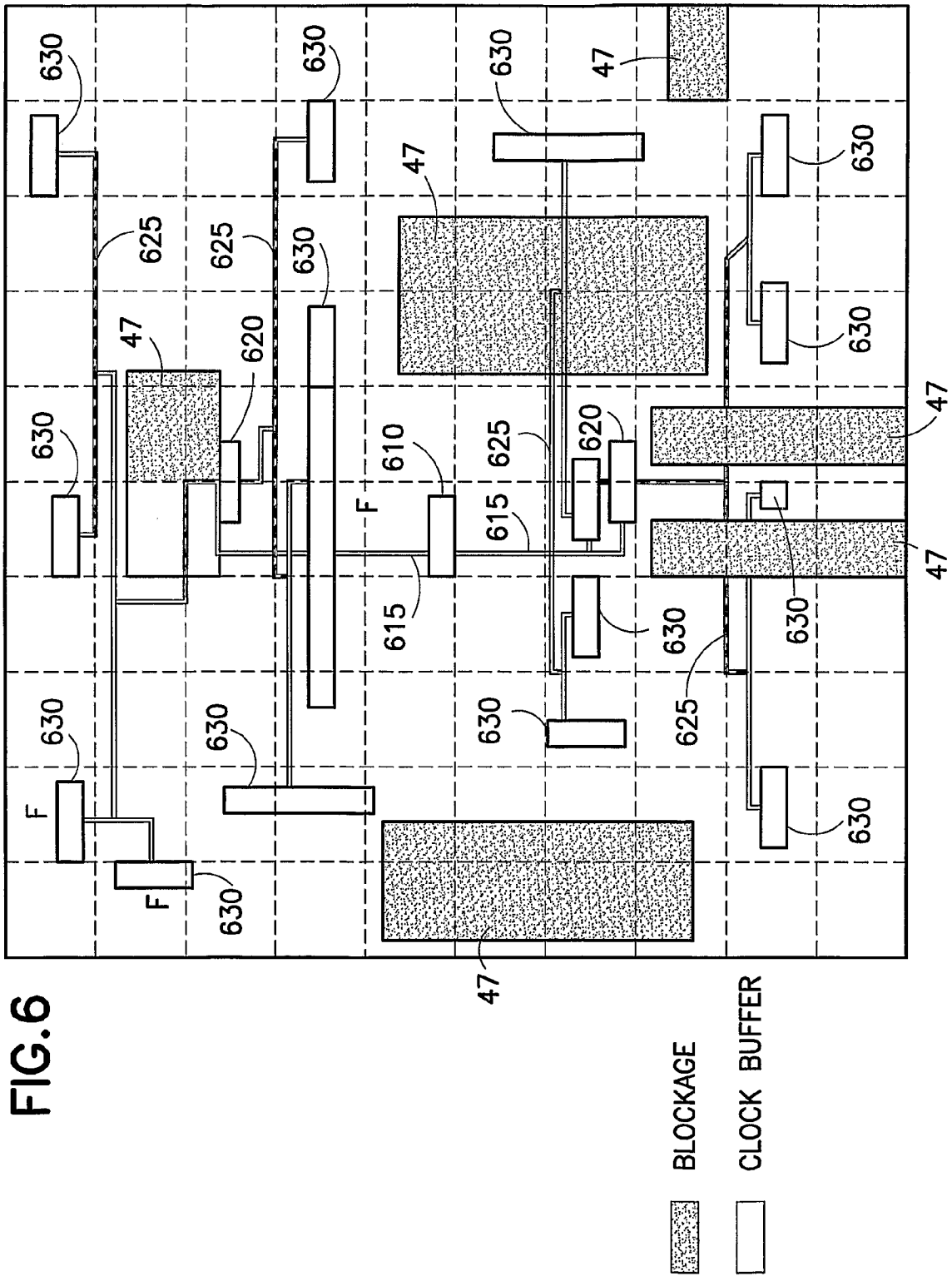


FIG.6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/40428

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 17/50
US CL : 716/1, 2, 7

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 716/1, 2, 7

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,849,610 A (Zhu) 15 December 1998 (15.12.1998), column 3, lines 10-17; column 6, lines 27-64; column 9, lines 12-67; column 10, lines 1-55; Figs. 2-9.	1
A	US 5,866,924 A (Zhu) 02 February 1999 (02-02-1999) whole document.	1-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2003 (20.03.2003)	09 JUN 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Matthew Smith Telephone No. (703) 308-1782

Deborah P. Vega
Paralegal Specialist
Technology Center 2800
(703) 308-3078

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

PCT/US02/40428

Continuation of B. FIELDS SEARCHED Item 3:
EAST; IEEE
clock adj tree; (cluster$3 or group$3) adj4 sink; symmetr$6 or (balanc$3 same (clock adj tree); root or souce; centroid or center; hiearch$6.